IN THE CLAIMS

Please amend the claims as follows.

For the Examiner's convenience, a list of all claims is included below.

1-11 (Canceled)

12. (Currently Amended) A flash memory cell comprising:

a plurality of gate stacks formed on a substrate, and a plurality of active regions formed in the substrate, wherein each of the plurality of the gate stacks has a gate stack length and a gate stack width;

an interlayer dielectric (ILD) deposited over the gate stacks and the active regions;

a ~~single~~ one-dimensional slot patterned in the ILD, wherein the one dimensional slot is to provide access to the plurality of active regions; and

a bit line formed in the ~~single~~ slot, wherein the bit line is to contact the plurality of active regions through the slot, wherein the one-dimensional slot has a length along the length of the bit line that is substantially larger than a width that is the gate stack width.

13. (Original) The flash memory cell of claim 12, wherein the bit line comprises a tungsten plug.

14. (Original) The flash memory cell of claim 12, wherein the flash memory cell is a NOR memory cell.

15. (Original) The flash memory cell of claim 12, further comprising:

a plurality of nitride spacers adjacent to the gate stacks.

16. (Original) The flash memory cell of claim 12, wherein the gate stacks comprise a control gate and a floating gate.

17. (Previously Presented) The flash memory cell of claim 16, further comprising a word line to control the control gate.

18-22 (Canceled)

23. (Previously Presented) A nonvolatile memory device comprising:

a plurality of gate stacks formed on a substrate, wherein an etch stop layer forms a top surface of each gate stack within the plurality;

a plurality of active regions formed in the substrate;

an interlayer dielectric (ILD) deposited on the plurality of gate stacks and on the plurality of active regions;

a one-dimensional slot patterned in the ILD providing access to the plurality of active regions; and

a bit line formed in the slot, the bit line in contact with the top surface of the gate stacks and in contact with the plurality of active regions.

24. (Previously Presented) The nonvolatile memory device of claim 23, wherein the bit line comprises a tungsten plug.

25. (Previously Presented) The nonvolatile memory device of claim 23, wherein the gate stack has at least one silicide layer.

26. (Previously Presented) The nonvolatile memory device of claim 23, wherein the etch stop layer is a dielectric material.

27. (Previously Presented) The nonvolatile memory device of claim 26, wherein the dielectric material is a nitride.

28. (Previously Presented) The nonvolatile memory device of claim 23, wherein the etch stop layer is on e a silicide layer.

29. (Previously Presented) The nonvolatile memory device of claim 23, wherein a nitride spacer is adjacent to each of the plurality of gate stacks.

30. (Currently Amended) A nonvolatile memory device comprising:

a plurality of gate stacks formed on a substrate, wherein each gate stack within the plurality comprises an etch stop layer;

a plurality of active regions formed in the substrate;

an interlayer dielectric (ILD) on the plurality of active regions and on and adjacent to each gate stack of the plurality of gate stacks and;

a bit line formed in [[the]] a slot, the bit line in contact with the etch stop layer of the plurality of gate stacks and in contact with the plurality of active regions.

31. (Previously Presented) The nonvolatile memory device of claim 30, wherein the bit line comprises a tungsten plug.

32. (Previously Presented) The nonvolatile memory device of claim 30, wherein the gate stack has at least one silicide layer.

33. (Previously Presented) The nonvolatile memory device of claim 30, wherein the etch stop layer is a dielectric material.

34. (Previously Presented) The nonvolatile memory device of claim 33, wherein the dielectric material is a nitride.

35. (Previously Presented) The nonvolatile memory device of claim 30, wherein the etch stop layer is on a silicide layer.

36. (Previously Presented) The nonvolatile memory device of claim 30, wherein a nitride spacer is adjacent to each of the plurality of gate stacks.